18. (Original) The integrated circuit as defined in claim 12 further comprising:

a sense amplifier having an input coupled to the read bit line; and

a multiplexer coupled between an output of the sense amplifier and the write bit line.

19. (Currently Amended) A method for controlling programmable interconnects and logic functions ~~storing data in and accessing data~~ from a DRAM cell, the method comprising:

applying a first voltage on a write word line to turn on a first transistor;

applying a second voltage on a write bit line coupled to a drain of the first transistor to store charge at a gate of a second transistor, a capacitor being coupled to the gate of the second transistor to store a charge at the gate of the second transistor;

applying a third voltage on the write word line to turn off the first transistor; and

directly driving a gate voltage of a pass gate using the charge stored on the capacitor,

~~applying a fourth voltage on a read word line to turn on a third transistor, wherein the second transistor is coupled in series with third transistor; and~~

~~sensing a fifth voltage on a read bit line coupled to a drain of the third transistor, the second and third transistors conducting current between the read bit line and a supply voltage if the charge stored at the gate of the second transistor is a first logic state,~~

wherein the write word line is not directly connected to the read word line.

Claim 20. (Canceled)

21. (Currently Amended) The method according to claim 19, further comprising:

applying a fourth voltage on a read word line to turn on a third transistor, wherein the second transistor is coupled in series with third transistor; and